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10/541,275	06/30/2005	Orlando Miguel Pires Dos Reis Moreira	260686	6275

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EXAMINER	
VICARY, KEITH E	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/541,275	PIRES DOS REIS MOREIRA ET AL.	
	Examiner	Art Unit	
	Keith Vicary	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/30/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-29 are pending in this office action and presented for examination. Claims 5, 7, 15, 18, 23-24, and 27-28 are newly amended by preliminary amendment filed 6/30/2005 which eliminated any multiple dependencies.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

3. Claims 1, 8, 13-14, and 23 are objected to because of the following informalities. Appropriate correction is required.

4. Claim 1, lines 1-2, recites the limitation "element" which should presumably be "elements".

5. Claim 1, line 5, contains a misplaced space by the comma. Also see claim 8.

6. Claim 13 appears to have an extra space in the second line. Also see claim 14.

7. Claim 23 recites the limitation "the memory consisting of" in line 2, which should be worded in a slightly different manner, for example, "wherein the memory consists of".

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 1 recites the limitation "tasking units which task units comprise" in line 4 which should be reworded for clarity purposes. Also see claim 29, which discloses in lines 4-5 of "according to which method".

a. Claims 2-28 are rejected for failing to alleviate the rejection of claim 1 above.

11. Claim 7 recites the limitation "the common control signal" in line 2. There is insufficient antecedent basis for this limitation in the claim.

b. Claims 8-23 are rejected for failing to alleviate the rejection of claim 7 above.

12. Claim 9 recites the limitation "the combination elements" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

13. Claim 10 recites the limitation "the channel infrastructure" in lines 1-2, as opposed to "the reconfigurable channel infrastructure". There is insufficient antecedent basis for this limitation in the claim.

14. Claim 11 recites the limitation "the channel infrastructure" in lines 1-2, as opposed to "the reconfigurable channel infrastructure". There is insufficient antecedent basis for this limitation in the claim.

15. Claim 12 recites the limitation "the channel infrastructure" in lines 1-2, as opposed to "the reconfigurable channel infrastructure". There is insufficient antecedent basis for this limitation in the claim.

c. Claims 13-14 are rejected for failing to alleviate the rejection of claim 12 above.

16. Claim 13 recites the limitation "the combination elements in chains" in line 3. There is insufficient antecedent basis for this limitation in the claim.

d. Claim 14 is rejected for failing to alleviate the rejection of claim 13 above.

17. Claim 15 recites the limitation "the channel infrastructure" in line 2, as opposed to "the reconfigurable channel infrastructure". There is insufficient antecedent basis for this limitation in the claim.

e. Claims 16-23 are rejected for failing to alleviate the rejection of claim 15 above.

18. Claim 24 recites the limitation "the processing elements comprise VLIW processors" in lines 2-3. It is indefinite as to whether the processing elements as a whole or a part of a whole make up a VLIW processor, or whether *each* single processing element can execute a VLIW instruction. For the purposes of this office action and based on the instant specification, examiner is assuming that it is the former case.

f. Claims 25-27 are rejected for failing to alleviate the rejection of claim 24 above.

19. Claim 26 recites the limitation "the interconnect network" in line 2, as opposed to "the internal interconnect network". There is insufficient antecedent basis for this limitation in the claim. Also see claim 27.

20. Note that claims 6 and 28 are rejected a second time using an additional art in a manner which more specifically reads on the instant application for the purposes of further prosecution.

Claim Rejections - 35 USC § 102

21. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

22. Claims 1-8, 12-15, 18-22, and 24-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Gove et al. (Gove) (US 5212777).

23. Consider claims 1 and 29, Gove discloses a processing system comprising a plurality of processing element (col. 3, lines 5-6. plurality of processors), the processing elements comprising a controller and computation means (col. 61, lines 28-29 for example, each processing element consists of...the controller and datapath), the plurality of processing elements being dynamically reconfigurable as mutually independently operating task units which task units comprise one processing element or

a cluster of two or more processing elements, the processing elements within a cluster being arranged to execute instructions under a common thread of program control (col. 3, lines 5-20, arranging a group of the processors into the SIMD operating mode with circuitry operable on a processor cycle by cycle basis for changing at least some of the processors from the group of processors from operation in the SIMD operating mode to operation in the MIMD operational mode; also note col. 62, lines 40-52, which discloses that many variations are possible including synchronized MIMD and that any number of the processors could be allocated to any of the modes).

24. Consider claim 2, Gove discloses that processing elements organized in a task unit share at least one common control signal for controlling instruction execution (Figure 22, the SYNC'D signals for example, which are distributed to elements in each task unit which control instruction execution; or the executed signal which each processing unit has when the limitation is interpreted in the same way as the instant specification. Additionally, Figure 4 when an SIMD mode is specified and each processing element fetches from the same instruction memory).

25. Consider claim 3, Gove discloses of conditional branch instructions in, for example, col. 50, lines 49-60. The overall invention of Gove supports the execution of conditional branches in either the SIMD or the synchronized MIMD mode; therefore, the signal which enable or carry out those modes as disclosed above control the conditional jump.

26. Consider claim 4, Gove discloses of conditional branch instructions in, for example, col. 50, lines 49-60. The overall invention of Gove supports the execution of conditional branches in either the SIMD or the synchronized MIMD mode; therefore, the signal which enable or carry out those modes as disclosed above control the conditional jump.

27. Consider claim 5, Gove discloses that the processing elements are connected to each other via data-path connections (DPC) (Figure 22).

28. Consider claim 6, Gove discloses the data-path connections (DPC) are limited to neighbour-to-neighbour connections (Figure 22, each processing element can be considered a neighbour).

29. Consider claim 7, Gove discloses the common control signal is derived from intermediate control signals transmitted through a reconfigurable channel infrastructure connected to the processing elements (Figure 22, wherein the common control signal is the execution signal and is derived from the various other lines entering in the NAND gates from the processor elements).

30. Consider claim 8, Gove discloses he common control signal is derived by combining the intermediate control signals through a combination element, associated

to each processing element (Figure 22, wherein the common control signal is the execution signal and is derived from the various other lines entering in the NAND gates from the processor elements).

31. Consider claim 12, Gove discloses the channel infrastructure comprises mutually transverse chains (Figure 22, for example, chains 40 and the lines vertically connected to that chain; or the horizontal chain emanating from the NAND gate which is inputted the OK TO SYNC signal and the vertically connected lines which lead into the other group of NAND gates).

32. Consider claim 13, Gove discloses the intermediate control signals transmitted through chains having a first orientation are forwarded to the combination elements in chains having a second orientation (Figure 22, wherein the first orientation is horizontal from the OK TO SYNC NAND gate and the second orientation is vertical containing the other ground of NAND gates; alternatively, the results of the 4 parallel NAND gates are forwarded to another NAND gate that is perpendicular to the aforementioned results).

33. Consider claim 14, Gove discloses the intermediate control signals transmitted through the chains having the second orientation are forwarded to the combination elements in the chains having the first orientation (Figure 22, for example, where the vertically oriented NAND which is inputtted the OK TO SYNC signal traverses the SYNCD set of horizontal lines).

34. Consider claim 15, Gove discloses the channel infrastructure comprises combination elements for combining an intermediate control signal transmitted through the channel infrastructure with an operation control signal of associated processing elements (Figure 22, the NAND gates combine the SYNC'D signals with the sync control signals; alternatively, NAND results are NAND'd with other NAND results to obtain the execute signal), and programmable switches between pairs of processing elements (Figure 22, the sets of four parallel NAND gates), for locally controllably inhibiting transmission of intermediate control signals (Figure 22, depending on the sync control signals, intermediate control signals may be inhibited from causing execution).

35. Consider claim 18, Gove discloses the programmable switches are programmed by signals stored in memory cells (Figure 22, whether or not the NAND gates let through the SYNCd signal is dependent on how it is programmed by the sync control word, which is disclosed in col. 20, line 59, sync registers).

36. Consider claim 19, Gove discloses at least one of the processing elements can write to at least one of the memory cells (col. 22, lines 58-61, sync bits are set by software depending upon the desired synchronization between the various processors).

37. Consider claim 20, Gove discloses a set of memory cells used to program the switches is organized as a data-word in a memory (col. 20, line 59, each sync register with multi-bit contents can be considered a data-word).

38. Consider claim 21, Gove discloses the memory contains multiple data-words, and wherein the programmable switches are programmed by selecting one of these data-words (Figure 22 and col. 20, line 59, different switches are connected to different sync registers).

39. Consider claim 22, Gove discloses one or more of the processing elements can program the programmable switches by dynamically selecting the data-word in memory (col. 22, lines 58-61, sync bits are set by software depending upon the desired synchronization between the various processors).

40. Consider claim 24, Gove discloses the processing elements comprise VLIW processors (col. 62, lines 40-52, which discloses that many variations are possible including MIMD and synchronized MIMD).

41. Consider claim 25, Gove discloses the VLIW processors comprise an internal interconnect network (Figure 22; alternative, it is inherent that inside each processor element there exists an interconnect network, such as from the registers to an ALU and so forth).

42. Consider claim 26, Gove discloses the interconnect network consists of point-to-point connections (Figure 22, it is inherent a processor contains point-to-point connections; such as between sync control bit 0 and a NAND gate, and so forth).

43. Consider claim 27, Gove discloses the interconnect network (IN) comprises data-path connections (DPC) going across processing elements (Figure 22).

44. Consider claim 28, Gove discloses the processing elements are arranged in a 2-dimensional grid (Figure 22, each processor element is in effect part of a 2-dimensional grid).

45. Claims 9-11 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gove as applied to claims 8 and 15 above, and further in view of Belton (Basic Gate and Functions).

46. Consider claim 9, Gove does not explicitly disclose that the combination elements consist of OR-gates; as seen in Figure 22, NAND gates are used.

Although OR gates were very well known to one of ordinary skill in the art at the time of the invention, Belton explicitly discloses of NAND gates (page 3). Moreover, although the notion that, given desired inputs and outputs, many different combinational logic structures could be used to implement those inputs and outputs, Belton also

explicitly discloses that a function in sum of products form can be implemented using NAND gates by replacing all AND and OR gates by NAND gates (page 3, bottom).

It would have been obvious to one of ordinary skill in the art at the time of the invention that it would have been a design choice as to, given desired inputs and outputs, which specific combinational logic structure is used to implement the logic function.

47. Consider claim 10, Gove does not explicitly disclose the channel infrastructure comprises programmable sum-terms; as seen in Figure 22, NAND gates are used.

Although OR gates were very well known to one of ordinary skill in the art at the time of the invention, Belton explicitly discloses of NAND gates (page 3). Moreover, although the notion that, given desired inputs and outputs, many different combinational logic structures could be used to implement those inputs and outputs, Belton also explicitly discloses that a function in sum of products form can be implemented using NAND gates by replacing all AND and OR gates by NAND gates (page 3, bottom).

It would have been obvious to one of ordinary skill in the art at the time of the invention that it would have been a design choice as to, given desired inputs and outputs, which specific combinational logic structure is used to implement the logic function.

48. Consider claim 11, Gove does not explicitly disclose the channel infrastructure comprises programmable product-terms; as seen in Figure 22, NAND gates are used.

Although OR gates were very well known to one of ordinary skill in the art at the time of the invention, Belton explicitly discloses of NAND gates (page 3). Moreover, although the notion that, given desired inputs and outputs, many different combinational logic structures could be used to implement those inputs and outputs, Belton also explicitly discloses that a function in sum of products form can be implemented using NAND gates by replacing all AND and OR gates by NAND gates (page 3, bottom).

It would have been obvious to one of ordinary skill in the art at the time of the invention that it would have been a design choice as to, given desired inputs and outputs, which specific combinational logic structure is used to implement the logic function.

49. Consider claim 16, Gove does not explicitly disclose the combination elements consist of OR-gates; as seen in Figure 22, NAND gates are used.

Although OR gates were very well known to one of ordinary skill in the art at the time of the invention, Belton explicitly discloses of NAND gates (page 3). Moreover, although the notion that, given desired inputs and outputs, many different combinational logic structures could be used to implement those inputs and outputs, Belton also explicitly discloses that a function in sum of products form can be implemented using NAND gates by replacing all AND and OR gates by NAND gates (page 3, bottom).

It would have been obvious to one of ordinary skill in the art at the time of the invention that it would have been a design choice as to, given desired inputs and

outputs, which specific combinational logic structure is used to implement the logic function.

50. Consider claim 17, Gove does not explicitly disclose the programmable switches comprise AND-gates; as seen in Figure 22, NAND gates are used.

Although OR gates were very well known to one of ordinary skill in the art at the time of the invention, Belton explicitly discloses of NAND gates (page 3). Moreover, although the notion that, given desired inputs and outputs, many different combinational logic structures could be used to implement those inputs and outputs, Belton also explicitly discloses that a function in sum of products form can be implemented using NAND gates by replacing all AND and OR gates by NAND gates (page 3, bottom).

It would have been obvious to one of ordinary skill in the art at the time of the invention that it would have been a design choice as to, given desired inputs and outputs, which specific combinational logic structure is used to implement the logic function.

51. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gove as applied to claim 18 above.

52. Consider claim 23, Gove discloses of a sync bits which are located in a sync registers, and thus does not disclose that the sync bits are located in a volatile random access memory (RAM). Gove does disclose of data RAM (Figure 4, element 10) in general.

It would have been readily recognized to one of ordinary skill in the art at the time of the invention that it would have been a design choice as to whether to use a register or RAM to hold values due to the tradeoffs involves, such as speed versus cost.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the register of Gove with a RAM in order to result in cost savings.

Second rejection of claims 6 and 28

53. Claims 6 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gove as applied to claim 1 and 5 above, and further in view of Parcerisa et al. (Efficient Interconnects for Clustered Microarchitectures).

54. Consider claim 6, Gove does not explicitly disclose that the data-path connections are limited to neighbour-to-neighbour connections.

On the other hand, Parcerisa does disclose of a 2-dimensional mesh grid with inter-processor connections made to nearest-neighbor processors only (section 3.5, last parargraph, mesh).

A 2-dimensional mesh grid is desirable because delays are shorter, due to requiring shorter wires and having smaller parasitic capacitance, network cost is lower, and it is more scalable (Parcerisa, section 3.5, last paragraph).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Parcerisa with the invention of Gove because delays are shorter, due to requiring shorter wires and having smaller parasitic

capacitance, network cost is lower, and it is more scalable. It would have been readily recognized to one of ordinary skill in the art at the time of the invention that the invention of Gove is adaptable to account for the teachings of Parcerisa.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Parcerisa with the invention of Gove in order to map well to planar integrated circuits and maintain link communication at full clock rates.

55. Consider claim 28, Gove does not explicitly disclose the processing elements are arranged in a 2-dimensional grid.

On the other hand, Parcerisa does disclose of a 2-dimensional mesh grid with inter-processor connections made to nearest-neighbor processors only (section 3.5, last parargraph, mesh).

A 2-dimensional mesh grid is desirable because delays are shorter, due to requiring shorter wires and having smaller parasitic capacitance, network cost is lower, and it is more scalable (Parcerisa, section 3.5, last paragraph).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Parcerisa with the invention of Gove because delays are shorter, due to requiring shorter wires and having smaller parasitic capacitance, network cost is lower, and it is more scalable. It would have been readily recognized to one of ordinary skill in the art at the time of the invention that the invention of Gove is adaptable to account for the teachings of Parcerisa.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Parcerisa with the invention of Gove in order to map well to planar integrated circuits and maintain link communication at full clock rates.

Conclusion

56. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

g. IBM (IBM Technical Disclosure Bulletin, September 1981, US; NN81091837) discloses of a PLA Logic Reduction Technique.

h. IBM (IBM Technical Disclosure Bulletin, March 1986, US; NN86034677) discloses of removing redundancies from Programmable Logic Arrays.

i. Kogge (US 5475856) discloses of a dynamic multi-mode parallel processing array.

j. Taylor et al. (US 5664214) discloses of combining the characteristics of both a SIMd and MIMD architecture into a single parallel processing computer.

k. Horstmann et al. (US 5774369) discloses of removing redundancies in logic networks.

l. Wilkinson et al. (US 5805915, 5828894, 5878241) discloses of a SIMIMD array processing system.

m. Pechanek et al. (US 6219776) discloses of a dynamic merged processor which has both SIMD and VLIW modes.

n. Jackson et al. (US 6487651) discloses of an MIMD arrangement of SIMD machines.

57. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith Vicary whose telephone number is (571)270-1314. The examiner can normally be reached on Monday - Thursday, 6:45 a.m. - 6:15 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

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